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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,049	07/28/2003	Young-Joon Choi	4591-343	5961

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EXAMINER	
RAHMAN, FAHMIDA	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,049	CHOI ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-10* is/are rejected.

7)☒ Claim(s) *5,6,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to arguments filed on 9/19/06.

2. Claim 2 has been amended, claims 13-18 have been canceled and no new claims have been added. Thus, claims 1-12 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Aizawa (US Patent Application Publication 2002/0039325).

For claim 1, applicant admitted in pages 1-2 that the following limitations are cited in prior art:

A computer system (Fig 1) comprising:

- a system controller (1 in Fig 1) including a central processing unit (5 in Fig 1) and a memory bus controller(7 in Fig 1) and configured to operate in a first interface mode;

- a system memory (3 in Fig 1) connected with the system controller (1) through the system bus (2 in Fig 1);
- a NAND flash memory (4 in Fig 1) configured to store a system driving code ("boot code" in lines 32-33 of page 1 in specification; "BS" in 9 of Fig 1), an operating system program ("OS" in 9 of Fig 1), and user data for the computer system ("UD" in 9 of Fig 1);
- and an interface unit (8 in Fig 1) configured to communicate with the system controller through the system bus in the first interface mode (controller 8 is configured to communicate with 1 through 2) and configured to communicate with the NAND flash memory in a second interface mode (8 is configured to operate with 9).

The following limitations are not explicitly mentioned in the applicant's admitted prior art:

- the interface unit being synchronized with a clock signal generated in response to predetermined command information.

However, the interface 8 must be synchronized with a clock signal, since the processing unit 1 is clock driven. The generation of clock signal needs to be associated with a predetermined command information. Thus, the limitation that the interface unit being synchronized with a clock signal generated in response to predetermined command information is inherent in AAPA.

In addition, Aizawa explicitly teaches the following limitations:

An interface unit (203) configured to communicate with the system controller (202) through the system bus (bus is shown as a vertical line between 203 and 202) in the first interface mode (the first interface mode is the mode where MPU communicates with 203) and configured to communicate with the flash memory (112) in a second interface mode (second interface mode is the mode where 203 communicates with 112) where an interface unit (203) is synchronized with a clock signal (CLK1) generated in response to predetermined command information (Q-OFF, CLK_ON, S_OFF).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of applicant's admission of prior art and Aizawa. One ordinary skill in the art would have been motivated to have a clock signal generated in response to predetermined command information, since it is not necessary to provide a continuous clock in the interface unit. The interface can be clocked only when it is accessed by the computer system and a significant power saving can be achieved by stopping the clock ([0007] in page 1 of Aizawa), since power consumption is related to clock speed.

For claim 7, Aizawa teaches the computer system with following limitations:

The interface unit comprises:

- a first interface unit configured to communicate with the system controller through the system bus in the first interface mode (203 interfaces with 202 through

system bus. Thus, it must have a first interface unit configured to communicate with the system controller 202);

- a second interface unit synchronized with the clock signal and configured to communicate with the flash memory in the second interface mode (203 comprises a second interface unit that communicates with 112 and 203 is synchronized with CLK1);
- a storage unit configured to store information and data exchanged between the first and second interface units (203 comprises clock signal, which means that 203 has a storage unit to store the necessary information and data) ;
- and a control unit synchronized with the clock signal and configured to control a transmission of the information and data between the first and second interface units (203 must control the interface between 202 and 112. Thus, it must comprise a control unit).

Aizawa does not teach that the flash memory is a NAND flash memory. However, AAPA teaches the NAND flash memory.

Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Aizawa (US Patent Application Publication 2002/0039325), further in view of Sassa (US Patent 6098077).

For claim 2, Aizawa's clock signal (CLK1) is generated from an oscillator (401) and a state machine controller (311) controls the inner operation of an IO interface (201). However, neither Aizawa nor AAPA provides the description of interface unit.

Sassa teaches a system wherein the interface unit (21 in Fig 2) comprises:

- a host interface unit (31) configured to communicate with the system controller (17) through the system bus (16) in the first interface mode (first interface mode is in between CPU and 21);
- a register unit (36) configured to store configuration information about the computer system, the NAND flash memory, and the command information;
- a buffer unit (32) for configured to store data of the NAND flash memory (22);
- an oscillator (37) configured to generate a clock signal to synchronize the interface unit ;
- a controller (33) synchronized with the clock signal and configured to control an inner operation of the interface unit in response to the command information ; and
- a NAND flash interface unit (21) synchronized with the clock signal and configured to communicate with the NAND flash memory (22) via the controller (33) in the second interface mode (second interface mode is in between 21 and 22).

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined teachings of applicant's admission of prior art and Aizawa in accordance with Sassa, since a NAND flash memory can't be accessed without proper interface unit. One ordinary skill in the art would have been motivated to have an interface unit as taught by Sassa, since the interface ensures reliable operation of NAND flash.

For claim 8, neither Aizawa nor AAPA provides the description of storage unit. Sassa teaches a system wherein the interface unit (21 in Fig 2) comprises:

- a register unit (36) configured to store configuration information about the computer system, the NAND flash memory, and the command information;
- a buffer unit (32) for configured to store data of the NAND flash memory (22);
- an oscillator (37) configured to generate a clock signal to synchronize the interface unit ;

Claims 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Aizawa (US Patent Application Publication 2002/0039325), further in view of Sassa (US Patent 6098077), further in view of Gibson et al (US Patent 6601167).

Applicant's admission of prior art, as modified by Aizawa and Sassa does not teach that the interface unit comprises a power up detector to apply a power-sensing signal.

Gibson et al teach a system comprising power up detector (30) to generate power good signal as shown in Fig 6.

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of applicant's admission of prior art, Kim and Gibson et al. One ordinary skill in the art would have been motivated to include power up detector, since boot data within flash memory should be loaded when the power supply generates proper operating voltages. The power up detector ensures that the power supply reaches appropriate voltage, which in turn ensures safe loading of boot code.

For claim 4, 34 of Sassa is the ECC.

Claims 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admission of prior art, in view of Aizawa (US Patent Application Publication 2002/0039325), further in view of Gibson et al (US Patent 6601167).

For claim 9, Applicant's admission of prior art, as modified by Aizawa and Sassa does not teach that the interface unit comprises a power up detector to apply a power-sensing signal.

Gibson et al teach a system comprising power up detector (30) to generate power good signal as shown in Fig 6.

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of applicant's admission of prior art, Kim and Gibson et al. One ordinary skill in the art would have been motivated to include power up detector, since boot data within flash memory should be loaded when the power supply generates proper operating voltages. The power up detector ensures that the power supply reaches appropriate voltage, which in turn ensures safe loading of boot code.

For claim 10, 34 of Sassa is an ECC.

Allowable Subject Matter

Claims 5-6 and 11-12 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed on 9/19/06 have been fully considered but they are not persuasive.

Applicant argues that AAPA and Aizawa fail to teach an interface unit configured for first and second interface modes. Applicant further argues that AAPA teaches a single interface mode.

Examiner disagrees. Since applicant did not define interface mode in claim, 8 can be considered to have two interface modes. Fig 1 of AAPA shows interface unit 8 is communicating with 9 and 1. 9 and 1 are two different interfaces for 8. The first mode is the mode when 8 is communicating with 1 and second mode is when 8 is communicating 9. In the first mode, 8 has to communicate with 1 for commands/data that are specific to 1 and in second mode, 8 has to communicate with 9 for commands/data that are specific to 9. Similarly, 203 in Aizawa's system communicates with 202 and 112 in two interface modes, as the interfaces 202 and 112 are different and works with different signals.

Applicant further argues that Aizawa makes no mention of what interface means are used to interface MPU and the memory core.

Examiner disagrees. There is no requirement in claim about the type of interface means. As 112 and 202 are two different interfaces for 203, both 112 and 202 have their own mode to communicate with 203.

Applicant further argues that 203 does not comprise two interface units.

Examiner disagrees. 203 communicates with 112 and 202. Therefore, 203 has part of circuitry that sends necessary signals to 112. Fig 1 shows that a first bus connects 203 with 112. The first bus is part of one interface unit. A second bus connects 203 with 202. The second bus is part of another interface unit. As long as, two interfaces 112 and 202 are different, there are two interface units in 203 to communicate with the two interfaces.

Applicant further argues that Sassa does not teach a NAND flash interface unit as recited because it can't teach that an element comprises another element and simultaneously is that other element.

Examiner disagrees. 21 comprises a number of elements that interfaces with flash memory via controller 33. Therefore, 21, being the interface unit, comprises NAND interface unit. For now, 32, the buffer unit, can be thought as NAND flash interface unit too as it is communicating with NAND via controller 33.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116